Chettinad College of Engineering & Technology
Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai.

Department of Computer Science and Engineering

CS8491-COMPUTER ARCHITECTURE

Unit III - MCQ Bank

1. A clocking scheme in which all state changes occur on a clock edge is known as_____.

   A. edge-triggered clocking

   B. clocking methodology

   C. control signal

   D. None of the above.

   ANSWER: (A).

2. The approach used to determine when data is valid and stable relative to the clock is known as_____.

   A. edge-triggered clocking

   B. clocking methodology

   C. control signal

   D. None of the above.

   ANSWER: (B).

3. Signal used for multiplexor selection or for directing the operation of a functional unit; contrasts with a data signal, which contains information that is operated on by a functional unit is called as _____.

   A. edge-triggered clocking

   B. clocking methodology

   C. control signal

   D. None of the above.

   ANSWER: (C).

4. In clocking methodology, the signal is logically high or true is known as _____.

   A. edge-triggered clocking

   B. Control signal

   C. asserted

D. None of the above.

ANSWER: (C).

5. In clocking methodology, the signal is logically low or false is known as _____.

A. edge-triggered clocking

B. Control signal

C. asserted

D. deasserted

ANSWER: (D).

6. The address specified in a branch, which becomes the new program counter (PC.if the branch is taken is known as_____.

A. branch target address

B. sign extend

C. branch taken

D. branch not taken

ANSWER: (A).

7. A branch where the branch condition is satisfied and the program counter (PC. becomes the branch target.

A. branch target address

B. sign extend

C. branch taken

D. branch not taken

ANSWER: (C).

8. The field that denotes the operation and format of an instruction.

A. Opcode

B. Operand

C. Operator

D. sign extend

ANSWER: (A).

9. There are situations in pipelining when the next instruction cannot execute in the following clock cycle. These events are called hazards.

A. True

B. False

ANSWER: (A).

10. When a planned instruction cannot execute in the proper clock cycle because the hardware does not support the combination of instructions that are set to execute.

A. structural hazard

B. data hazards

C. control hazards

D. hazards

ANSWER: (A).

11. A method of resolving a data hazard by retrieving the missing data element from internal buffers rather than waiting for it to arrive from programmer visible registers or memory.

A. structural hazard

B. data hazards

C. control hazards

D. bypassing

ANSWER: (D).

12. Pipeline stall is also called bubble.

A. True

B. False

ANSWER: (A).

13. A method of resolving a branch hazard that assumes a given outcome for the branch and proceeds from that assumption rather than waiting to ascertain the actual outcome.

A. branch prediction

B. branch history table

C. prediction

D. branch delay

ANSWER: (A).

14. A small memory that is indexed by the lower portion of the address of the branch instruction and that contains one or more bits indicating whether the branch was recently taken or not.

A. branch prediction

B. branch history table

C. prediction

D. branch delay

ANSWER: (B).

15. The slot directly after a delayed branch instruction, which in the MIPS architecture is filled by an instruction that does not affect the branch.

A. branch delay slot

B. branch prediction

C. branch history table

D. prediction

ANSWER: (A).

16. Vectored interrupt is an interrupt for which the address to which control is transferred is determined by the cause of the exception.

A. True

B. False

ANSWER: (A).

17. An interrupt or exception that is always associated with the correct instruction in pipelined computers.

A. Precise exception

B. Imprecise exception

C. Exception

D. Vector interrupt

ANSWER: (A).

18. An approach to implementing a multiple-issue processor where many decisions are made by the compiler before execution.

A. static multiple issue

B. dynamic multiple issue

C. speculation

D. loop delay

ANSWER: (A).

19. Which of the following is not a Pipeline Conflicts?

A. Timing Variations

B. Branching

C. Load Balancing

D. Data Dependency

ANSWER: (C).

20. Which of the following is disadvantage of Pipelining?

A. Cycle time of the processor is reduced.

B. The design of pipelined processor is complex and costly to manufacture.

C. The instruction latency is more.

D. Both B and C

ANSWER: (D).

21. In Arithmetic Pipeline, the floating point addition and subtraction is done in _____ parts.

A. 2

B. 3

C. 4

D. 5

ANSWER: (C).

22. The periods of time when the unit is idle is called as _____

A. Stalls

B. Bubbles

C. Hazards

D. Both Stalls and Bubbles

ANSWER: (D).

23. The situation wherein the data of operands are not available is called _____

A. Data hazard

B. Stock

C. Deadlock

D. Structural hazard

ANSWER: (A).

24. An approach to implementing a multiple issue processor where many decisions are made during execution by the processor.

A. static multiple issue

B. dynamic multiple issue

C. speculation

D. loop delay

ANSWER: (B).

25. A style of instruction set architecture that launches many operations that are defined to be independent in a single wide instruction, typically with many separate opcode fields.

A. Very Long Instruction Word (VLIW)

B. static multiple issue

C. dynamic multiple issue

D. speculation

ANSWER: (A).